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LMT070DICFWD-NJA

LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	Preliminary	2015-07-15
0.2	Typing correction	2016-04-05
0.3	Update 5.1 describe	2016-11-23
0.4	Update section 2,7	2018-2-7
0.5	Add section 3.2	2023-04-01

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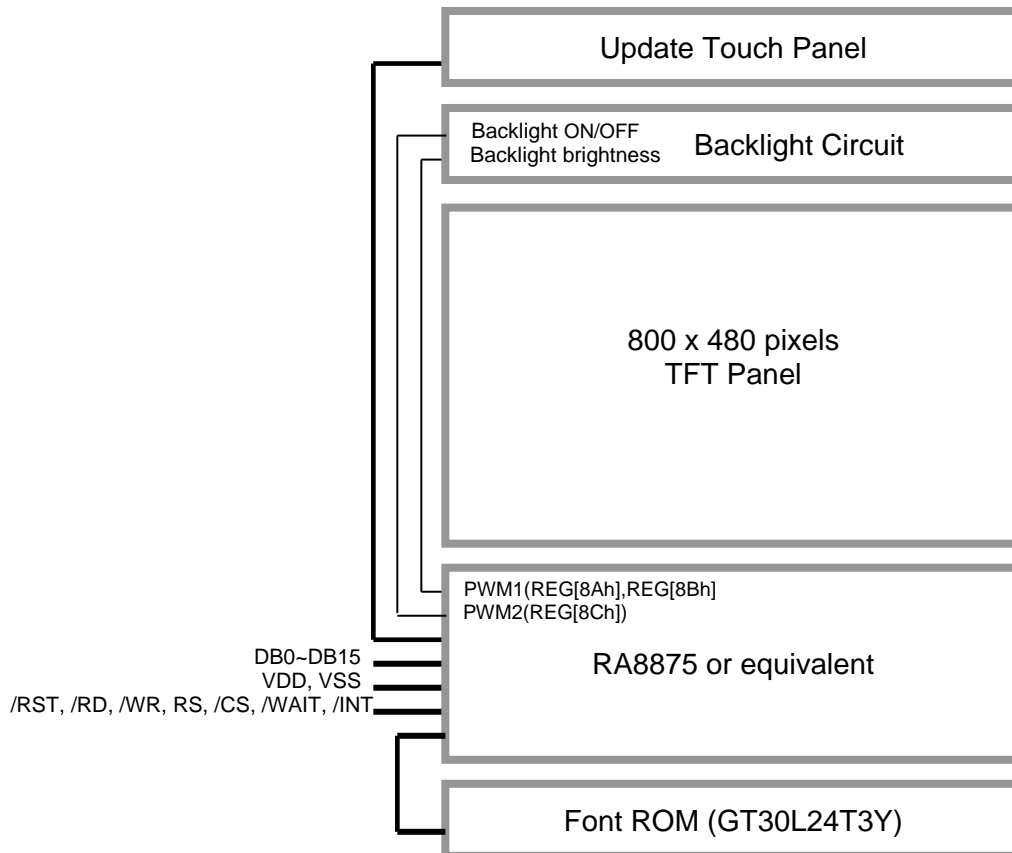
1. General Specification

Screen Size(Diagonal) :	7.0"
Outline Dimension :	190.0 x 112.0x 13.3max (mm) (see attached drawing for details)
Active Area :	154.08 x 85.92 (mm)
Color Depth:	65k
Number of dots :	800 x 480
Pixel Pitch :	0.0642 x0.179 (mm)
Pixel Configuration :	RGB Stripe
Backlight :	LED
Surface Treatment :	Anti-Glare Treatment
Viewing Direction :	6H (gray scale inverse)(*2) 12H(*3)
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:

- *1 Color tune may slightly changed by temperature and driving voltage.
- *2. For saturated color display content (eg. pure-red, pure-green, pure-blue, or pure-colors-combinations)
- *3. For "color scales" display content

2. Block Diagram



3. Terminal Functions

3.1 Interface(K1)

Pin No.	Pin Name	I/O	Descriptions	Note
1	VSS(0V)	P	Power Ground	
2	VDD(5.0V)	P	Positive Power Supply	
3	VDD(5.0V)			
4	RS	I	Register Select RS = H, status read/command write cycle is selected. RS = L, data Read/Write cycle is selected.	
5	/WR	I	/WR=L→H, RD=H; Data or Instruction latch into the LCD module	
6	/RD	I	/WR=H, /RD=L; Data or Status read form the LCD module	
7	/CS	I	Chip Select /CS=L, enable access to the LCD interface /CS=H, disable access to the LCD interface	
8	VSS(0V)	P	Power Ground	
9	/WAIT	O	Controller busy signal output, MCU should poll this signal before accessing the LCD module	
10	/INT	O	Interrupt signal output	
11	/RST	I	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.	
12	DB0	I	Data Input	
:	:	:	:	
19	DB7	I	Data Input	
20	VSS(0V)	P	Power Ground	
21	VDD(5.0V)	P	Positive Power Supply	
22	VSS(0V)	P	Power Ground	
23	DB8	I	Data Input	
:	:	:	:	
30	DB15	I	Data Input	

3.2 Interface(K2)

Pin No.	Pin Name	I/O	Descriptions	Note
1	VDD(5.0V)	P	Positive Power Supply	
2	VDD(5.0V)			
3	VDD(5.0V)			
4	VDD(5.0V)			
5	VSS(0V)	P	Power Ground	
6	VSS(0V)			
7	/WR	I	/WR=L→H, RD=H; Data or Instruction latch into the LCD module	
8	/RD	I	/WR=H, /RD=L; Data or Status read form the LCD module	
9	/CS	I	Chip Select /CS=L, enable access to the LCD interface /CS=H, disable access to the LCD interface	
10	RS	I	Register Select RS = H, status read/command write cycle is selected. RS = L, data Read/Write cycle is selected.	
11	DB15	I	Data Input	
:	:	:	:	
26	DB0	I	Data Input	
27	VSS(0V)	P	Power Ground	
28	VSS(0V)			
29	/INT	O	Interrupt signal output	
30	/WAIT	O	Controller busy signal output, MCU should poll this signal before accessing the LCD module	
31	NC	-	No connection	
32	/RST	I	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.	
33	NC	-	No connection	
34	NC			
35	VSS(0V)	P	Power Ground	
36	VSS(0V)			

4. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V _{DD}	-0.3	+7.0	V	GND = 0V
Operating Temperature	T _{OP}	-20	+70	°C	No Condensation
Storage Temperature	T _{ST}	-30	+80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

5. Electrical Characteristics

5.1 DC Characteristics (MCU terminal)

VDD=5.0V, VSS=0V, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	VDD	4.7	5.0	5.3	V	VDD
Input High Voltage	V _{IH}	3.0V	-	3.3	V	/RD, /WR, RS, /CS,
Input Low Voltage	V _{IL}	VSS	-	0.5	V	DB0~DB15, /RST
Output Signal High Voltage	V _{OH}	-	-	3.3	V	DB0~DB15, /WAIT, /INT
Output Signal Low Voltage	V _{OL}	VSS	-	-	V	
Operating Current	I _{DD}	-	350	-	mA	All black, Backlight ON (*1)
		-	120	-	mA	All black, Backlight OFF(*2)

Note:

*1.REG[8Ch]=40H For Backlight ON.

*2.REG[8Ch]=00H For Backlight OFF.

*3.REG[8Ah]=85H , REG[8Bh]=00H-FFH For Backlight brightness PWM Duty (3.7kHz PWM Freq.) .

6. AC Characteristics

6.1 AC Timing

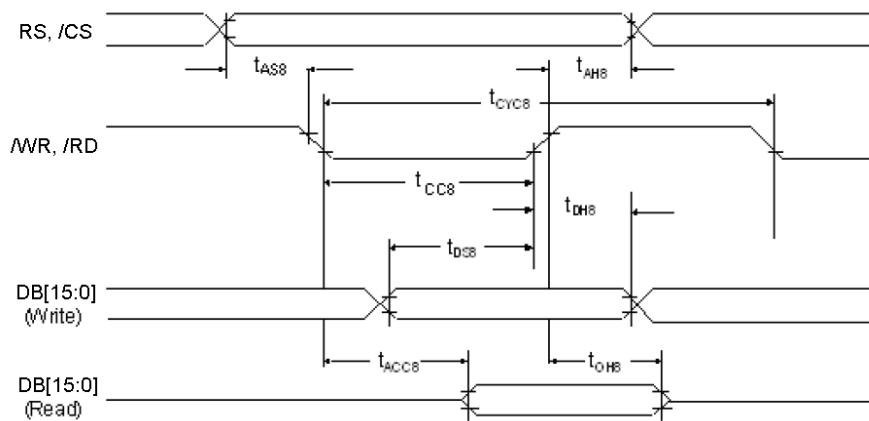
VDD=5.0V, VSS=0V, TOP =25°C

Parameter	Symbol	Spec.			Unit	Description
		Min.	Typ	Max.		
Cycle time	t _{CYC8}	71	-	-	ns	tc is one system clock period: tc = 1/SYS_CLK
Strobe Pulse width	t _{CCC8}	28	-	-		
Address setup time	t _{AS8}	5	-	-		
Address hold time	t _{AH8}	14	-	-		
Data setup time	t _{DS8}	28	-	-		
Data hold time	t _{DH8}	14	-	-		
Data output access time	t _{ACC8}	0	-	14		
Data output hold time	t _{OH8}	0	-	14		

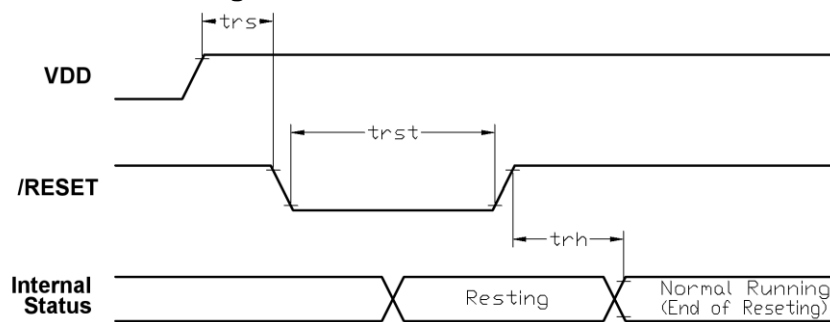
Note:1. Refer to the RA8875 datasheet for more details.

2. SYS_CLK (System clock) = 30MHz

Register Write/Read timing (for CPU 16 Bit)



6.2 TFT Controller Reset Timing



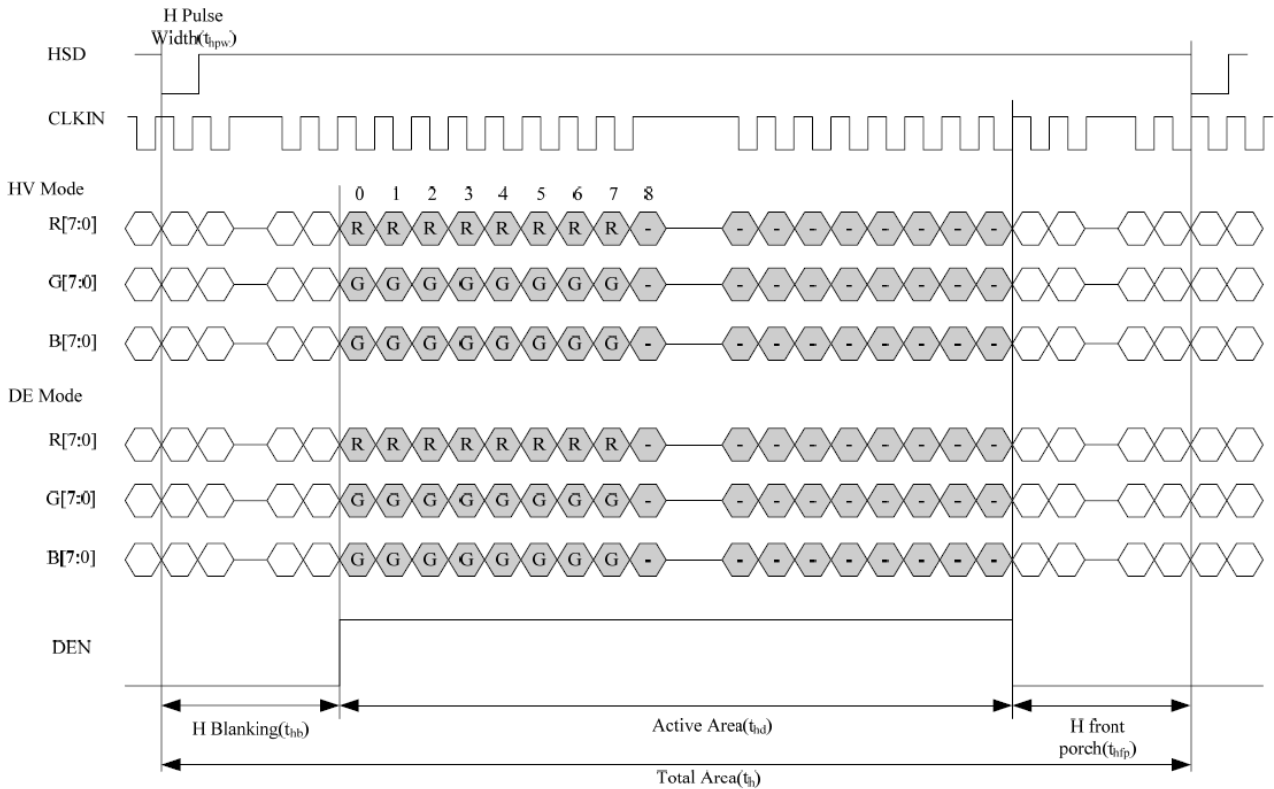
VSS=0V, VDD=5.0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset setup time	trs	2	-	-	ms
Reset pulse	trst	0.2	-	-	ms
Reset hold time	trh	2	-	-	ms

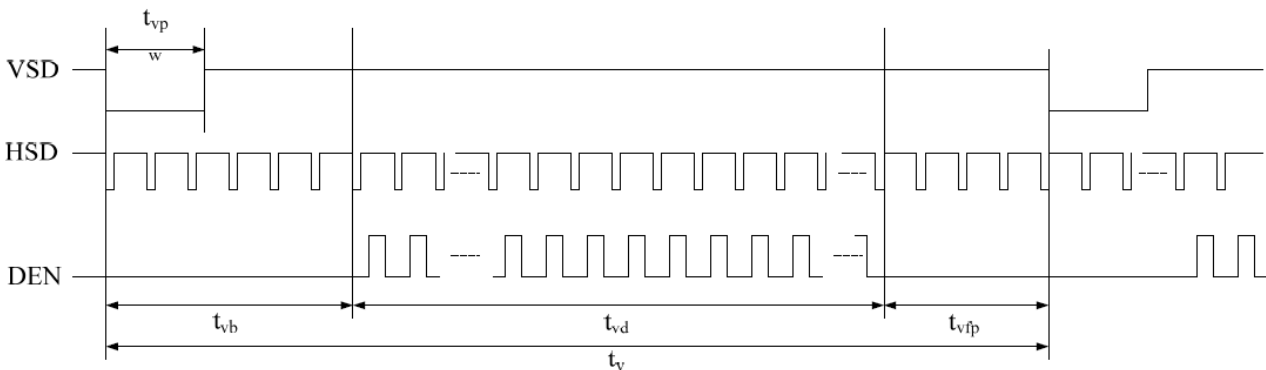
6.3 Panel Setting of Timing

Parameter	Symbol	Spec			Unit	Remark
		MIN.	TYP.	MAX.		
Horizontal Display Area	thd	-	800	-	CLKIN	
CLKIN Frequency(60HZ)	fclk	-	30	50	MHZ	
One Horizontal Line	th	889	928	1143	CLKIN	
HSD pulse width	thpw	1	48	255	CLKIN	
HSD Blanking	thb	88			CLKIN	
HSD Front Porch	thfp	1	40	255	CLKIN	
Vertical Display Area	tvd	480			TH	
VSD period time	tv	513	525	767	TH	
VSD pulse width	tvpw	3	3	255	TH	
VSD Blanking(tvb)	tvb	32			TH	
VSD Front Porch(tvfp)	tvfp	1	13	255	TH	

Horizontal Input Timing Diagram



Vertical Input Timing Diagram



7. Commands

REG[01h] Power and Display Control Register (PWRR)

Bit	Description	Default	Access
7	LCD Display Off 0:display off. 1:display on.	0	RW
6-2	NA	0	RO
1	Sleep Mode 0:Normal mode. 1:Sleep mode. Note: 1. There are 3 ways to wake up from sleep mode: Touch Panel wake up,Key Scan wake up,Software wake up. 2. When using IIC, this function is not supported. 3. When using SPI, it has its particular steps to use this function, refer to section 6-1-2-3 please.	0	RW
0	Software Reset 0 : No action. 1 : Software Reset. Note: The bit must be set to 1 and then set to 0 to complete a software reset	0	WO

REG[02h] Memory Read/Write Command (MRWC)

Bit	Description	Default	Access
7-0	Write Function : Memory Write Data Data to write in memory corresponding to the setting of MWCR1[3:2].Continuous data write cycle can be accepted in bulk data write case. Read Function : Memory Read Data Data to read from memory corresponding to the setting of MWCR1[3:2]. Continuous data read cycle can be accepted in bulk data read case. Note that the first data read cycle is dummy read and need to be ignored.	--	RW

REG[04h] Pixel Clock Setting Register (PCSR)

Bit	Description	Default	Access
7	PCLK Inversion 0 : PDAT is fetched at PCLK rising edge. 1 : PDAT is fetched at PCLK falling edge.	0	RW
6-2	NA	0	RO
1-0	PCLK Period Setting pixel clock (PCLK) period setting. 00b: PCLK period = System Clock period. 01b: PCLK period = 2 times of System Clock period. 10b: PCLK period = 4 times of System Clock period. 11b: PCLK period = 8 times of System Clock period.	0	RW

REG[05h] Serial Flash/ROM Configuration Register (SROC)

Bit	Description	Default	Access
7	Serial Flash/ROM I/F # Select 0: Serial Flash/ROM 0 I/F is selected. 1: Serial Flash/ROM 1 I/F is selected.	0	RW
6	Serial Flash/ROM Address Mode 0: 24 bits address mode This bit must set to 0 for serial flash .	0	RW
5	Serial Flash/ROM Waveform Mode Mode 0. Mode 3.	0	RW
4-3	Serial Flash /ROM Read Cycle 00b: 4 bus → no dummy cycle 01b: 5 bus → 1 byte dummy cycle 1xb: 6 bus → 2 byte dummy cycle	0	RW
2	Serial Flash /ROM Access Mode 0: Font mode 1: DMA mode	0	RW
1-0	Serial Flash /ROM I/F Data Latch Mode Select 0xb: Single Mode 10b: Dual Mode 0. 11b: Dual Mode 1.	0	RW

REG[06h] Serial Flash/ROM CLK Setting Register(SFCLR)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Serial Flash/ROM Clock Frequency Setting 0xb: SFCL frequency = System clock frequency (When DMA enable and Color depth = 256 color) SFCL frequency = System clock frequency / 2) 10b: SFCL frequency = System clock frequency / 2 11b: SFCL frequency = System clock frequency / 4	0	RW

REG[10h] System Configuration Register (SYSR)

Bit	Description	Default	Access
7-4	N/A	0	RO
3-2	Color Depth Setting 00b : 8-bpp generic TFT, i.e. 256 colors. 1xb : 16-bpp generic TFT, i.e. 65K colors.	0	RW
1-0	MCUIF Selection 00b : 8-bit MCU Interface. 1xb : 16-bit MCU Interface.	0	RW

REG[12h] GPI

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	GPI[4:0] : General Purpose Input. KEY_EN = 0: General Purpose Input from pin KIN[4:0] KEY_EN = 1: NC	NA	RO

Note:KEY_EN : REG[C0h] bit 7

REG[13h] GPO

Bit	Description	Default	Access
7-4	NA	0	RO
3-0	GPO[3:0] : General Purpose Output KEY_EN = 0: General Purpose Output to KOUT[3:0] KEY_EN = 1: NC	0	RW

Note: KxY_EN : REG[C0h] bit 7

REG[14h] LCD Horizontal Display Width Register (HDWR)

Bit	Description	Default	Access
7	NA	0	RO
6-0	Horizontal Display Width Setting Bit[6:0] The register specifies the LCD panel horizontal display width in the unit of 8 pixels resolution. Horizontal display width(pixels) = (HDWR + 1)x8	0	RW

Note : HDWR must be set less than 64h because that the maximum horizontal display width is 800 pixels.

REG[15h] Horizontal Non-Display Period Fine Tuning Option Register (HNDFTR)

Bit	Description	Default	Access
7	DE Polarity 0 : high active. 1 : low active.	0	RW
6-4	NA	0	RO
3-0	Horizontal Non-Display Period Fine Tuning(HNDFT) [3:0] This register specifies the fine tuning for horizontal non-display period; it is used to support the SYNC mode panel. Each level of this modulation is 2-pixel.	0	RW

REG[16h] LCD Horizontal Non-Display Period Register (HNDR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Horizontal Non-Display Period(HNDP) Bit[4:0] This register specifies the horizontal non-display period. Horizontal Non-Display Period (pixels) =(HNDR + 1)x8+(HNDFTR/2+1)x2 + 2	0	RW

REG[17h] HSYNC Start Position Register (HSTR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	HSYNC Start Position[4:0] The starting position from the end of display area to the beginning of HSYNC. Each level of this modulation is 8-pixel. HSYNC Start Position(pixels) = (HSTR + 1)x8	0	RW

REG[18h] HSYNC Pulse Width Resister (HPWR)

Bit	Description	Default	Access
7	HSYNC Polarity 0 : Low active. 1 : High active.	0	RW
6-5	NA	0	RO
4-0	HSYNC Pulse Width(HPW) [4:0] The period width of HSYNC. HSYNC Pulse Width(pixels) = (HPW + 1)x8	0	RW

REG[19h] LCD Vertical Display Height Register (VDHR0)

Bit	Description	Default	Access
7-0	Vertical Display Height Bit[7:0] Vertical display Height(Line) = VDHR + 1	0	RW

REG[1Ah] LCD Vertical Display Height Register0 (VDHR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Display Height bit[8] Vertical Display Height(Line) = VDHR + 1	0	RW

Note : The VDHR must be set less than 1E0h, because the maximum vertical display height is 480.

REG[1Bh] LCD Vertical Non-Display Period Register (VNDR0)

Bit	Description	Default	Access
7-0	Vertical Non-Display Period Bit[7:0] Vertical Non-Display Period(Line) = (VNDR + 1)	0	RW

REG[1Ch] LCD Vertical Non-Display Period Register (VNDR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Non-Display Period bit[8] Vertical Non-Display Period(Line) = (VNDR + 1)	0	RW

REG[1Dh] VSYNC Start Position Register (VSTR0)

Bit	Description	Default	Access
7-0	VSYNC Start Position[7:0] The starting position from the end of display area to the beginning of VSYNC. VSYNC Start Position(Line) = (VSTR + 1)	0	RW

REG[1Eh] VSYNC Start Position Register (VSTR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	VSYNC Start Position[8] The starting from the end of display area to the beginning of VSYNC. VSYNC Start Position(Line) = (VSTR + 1)	0	RW

REG[1Fh] VSYNC Pulse Width Register (VPWR)

Bit	Description	Default	Access
7	VSYNC Polarity 0 : Low active. 1 : High active.	0	RW
6-0	VSYNC Pulse Width[6:0] The pulse width of VSYNC in lines. VSYNC Pulse Width(Line) = (VPWR + 1)	0	RW

REG[20h] Display Configuration Register (DPCR)

Bit	Description	Default	Access
7	Layer Setting Control 0 : One layer configuration is selected. 1 : Two layers configuration is selected.	0	RW
6-4	NA	0	RO
3	HDIR Horizontal Scan Direction, for n = SEG number. 0 : SEG0 to SEG(n-1). 1 : SEG(n-1) to SEG0.	0	RW
2	VDIR Vertical Scan direction, for n = COM number 0 : COM0 to COM(n-1). 1 : COM(n-1) to COM0.	0	RW
1-0	NA	0	RO

REG[21h] Font Control Register 0 (FNCR0)

Bit	Description	Default	Access
7	CGRAM/CGROM Font Selection Bit in Text Mode 0 : CGROM font is selected. 1 : CGRAM font is selected. Note: 1. The bit is used to select the bit-map source when text-mode is active(REG[40h] bit 7 is 1), when CGRAM is writing(REG[41h] bit 3-2 =01b), the bit must be set as "0". 2. When CGRAM font is select, REG[21h] bit 5 must be set as 1.	0	RW
6	NA	0	RO
5	External/Internal CGROM Selection Bit 0 : Internal CGROM is selected.(REG[2Fh] must be set 00h) 1 : External CGROM is selected. (REG[2Eh] bit6 &bit7 must be set 0)	0	RW
4-2	NA	0	RO
1-0	Font Selection for internal CGROM When FNCR0 B7 = 0 and B5 = 0, Internal CGROM supports the 8x16 character sets with the standard coding of ISO/IEC 8859- 1~4, which supports English and most of European country languages. 00b : ISO/IEC 8859-1. 01b : ISO/IEC 8859-2. 10b : ISO/IEC 8859-3. 11b : ISO/IEC 8859-4.	0	RW

REG[22h] Font Control Register1 (FNCR1)

Bit	Description	Default	Access
7	Full Alignment Selection Bit 0 : Full alignment is disable. 1 : Full alignment is enable.	0	RW
6	Font Transparency 0 : Font with background color. 1 : Font with background transparency.	0	RW
5	NA	0	RO
4	Font Rotation 0 : Normal. 1 : 90 degree display.	0	RW
3-2	Horizontal Font Enlargement 00b : X1. 01b : X2. 10b : X3. 11b : X4.	0	RW
1-0	Vertical Font Enlargement 00b : X1. 01b : X2. 10b : X3. 11b : X4.	0	RW

REG[23h] CGRAM Select Register (CGSR)

Bit	Description	Default	Access
7-0	CGRAM No. The setting of the number of the character in CGRAM. It's used to write the user-defined character bitmap data into CGRAM. 16 continuous data write cycles complete the bitmap writing of a 8x16 character. Note that the MWCR1 bit 3-2 must be set as 01b(CGRAM) first. And more than 16 data write cycles will loop back to the 1 st data and cover the bitmap.	0	RW

REG[24h] Horizontal Scroll Offset Register 0 (HOFS0)

Bit	Description	Default	Access
7-0	Horizontal Display Scroll Offset [7:0] The display offset of the horizontal direction, changing the value will cause the effect of scrolling at horizontal direction.	0	RW

REG[25h] Horizontal Scroll Offset Register 1 (HOFS1)

Bit	Description	Default	Access
7-3	NA	0	RO
2-0	Horizontal Display Scroll Offset [10:8] The display offset of the horizontal direction, changing the value will cause the effect of scrolling at horizontal direction.	0	RW

REG[26h] Vertical Scroll Offset Register 0 (VOFS0)

Bit	Description	Default	Access
7-0	Vertical Display Scroll Offset [7:0] The display offset of the vertical direction, changing the value will cause the effect of scrolling at vertical direction.	0	RW

REG[27h] Vertical Scroll Offset Register 1 (VOFS1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Vertical Display Scroll Offset [9:8] The display offset of the vertical direction, changing the value will cause the effect of scrolling at vertical direction.	0	RW

REG[29h] Font Line Distance Setting Register (FLDR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Font Line Distance Setting Setting the font character line distance when setting memory font write cursor auto move. (Unit: pixel)	0	RW

REG[2Ah] Font Write Cursor Horizontal Position Register 0 (F_CURXL)

Bit	Description	Default	Access
7-0	Font Write Cursor Horizontal Position[7:0] The setting of the horizontal cursor position for font writing.	0	RW

REG[2Bh] Font Write Cursor Horizontal Position Register 1 (F_CURXH)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Font Write Cursor Horizontal Position[9:8] The setting of the horizontal cursor position for font writing.	0	RW

REG[2Ch] Font Write Cursor Vertical Position Register 0 (F_CURYL)

Bit	Description	Default	Access
7-0	Font Write Cursor Vertical Position[7:0] The setting of the vertical cursor position for font writing.	0	RW

REG[2Dh] Font Write Cursor Vertical Position Register 1 (F_CURYH)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Font Write Cursor Vertical Position[8] The setting of the vertical cursor position for font writing.	0	RW

REG[2Eh] Font Write Type Setting Resister

Bit	Description	Default	Access			
7-6	Font Size Setting(* 1)	0	RW			
				Full Size	Half-Size	Variable Width
	00b			16x16	8x16	NX16
	01b			24x24	12x24	NX24
	1Xb(* 2)			32x32	16x32	NX32
Note: * 1 The font width indicated by "N" depends on the character code of the FONT. * 2 The command is invalid , GT30L24T3Y does not support size of 32x32 .						
5-0	Font to Font Width Setting 00h : Font width off 01h : Font to Font width = 1 pixel 02h : Font to Font width = 2 pixels : 3Fh : Font to Font width = 63 pixels	0	RW			

REG[2Fh] Serial Font ROM Setting

Bit	Description	Default	Access			
7-5	GT Serial Font ROM Select 000b: GT21L16TW / GT21H16T1W 001b: GT30L16U2W 010b: GT30L24T3Y / GT30H24T3Y 011b: GT30L24M1Z 100b: GT30L32S4W / GT30H32S4W	0	RW			
4-2	FONT ROM Coding Setting For specific GT serial Font ROM, the coding method must be set for decoding. 000b: GB2312 001b: GB12345/GB18030 010b: BIG5 011b: UNICODE 100b: ASCII 101b: UNI-Japanese 110b: JIS0208 111b: Latin/Greek/ Cyrillic / Arabic	0	RW			
1-0	ASCII / Latin/Greek/ Cyrillic / Arabic Latin	0	RW			
				ASCII	Latin/Greek/ Cyrillic	Arabic Latin
	00b			Normal	Normal	NA
	01b			Arial	Variable Width	Presentation forms-A
	10b			Roman	NA	Forms-B
11b	Bold	NA	NA			

REG[30h] Horizontal Start Point 0 of Active Window (HSAW0)

Bit	Description	Default	Access
7-0	Horizontal Start Print of active Window [7:0]	0	RW

REG[31h] Horizontal Start Point 1 of active Window (HSAW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal Start Point of Active Window [9:8]	0	RW

REG[32h] Vertical Start Point 0 of Active Window (VSAW0)

Bit	Description	Default	Access
7-0	Vertical Start Point of Active Window [7:0]	0	RW

REG[33h] Vertical Start Point 1 of Active Window (VSAW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Start Point of Active Window [8]	0	RW

REG[34h] Horizontal End Point 0 of Active Window (HEAW0)

Bit	Description	Default	Access
7-0	Horizontal End Point of Active Window [7:0]	0	RW

REG[35h] Horizontal End Point 1 of Active Window (HEAW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal End Point of Active Window [9:8]	0	RW

REG[36h] Vertical End Point of Active Window 0 (VEAW0)

Bit	Description	Default	Access
7-0	Vertical End Point of Active Window [7:0]	0	RW

REG[37h] Vertical End Point of Active Window 1 (VEAW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical End Point of Active Window [8]	0	RW

REG[38h] Horizontal Start Point 0 of Scroll Window (HSSW0)

Bit	Description	Default	Access
7-0	Horizontal Start Point of Scroll Window [7:0]	0	RW

REG[39h] Horizontal Start Point 1 of Scroll Window (HSSW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal Start Point of Scroll Window [9:8]	0	RW

REG[3Ah] Vertical Start Point 0 of Scroll Window (VSSW0)

Bit	Description	Default	Access
7-0	Vertical Start Point of Scroll Window [7:0]	0	RW

REG[3Bh] Vertical Start Point 1 of Scroll Window (VSSW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Start Point of Scroll Window [8]	0	RW

REG[3Ch] Horizontal End Point 0 of Scroll Window (HESW0)

Bit	Description	Default	Access
7-0	Horizontal End Point of Scroll Window [7:0]	0	RW

REG[3Dh] Horizontal End Point 1 of Scroll Window (HESW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal End Point of Scroll Window [9:8]	0	RW

REG[3Eh] Vertical End Point 0 of Scroll Window (VESW0)

Bit	Description	Default	Access
7-0	Vertical End Point of Scroll Window [7:0]	0	RW

REG[3Fh] Vertical End Point 1 of Scroll Window (VESW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical End Point of Scroll Window [8]	0	RW

REG[40h] Memory Write Control Register 0 (MWCR0)

Bit	Description	Default	Access
7	Text Mode enable 0 : Graphic mode. 1 : Text mode.	0	RW
6	Font Write Cursor/ Memory Write Cursor Enable 0 : Font write cursor/ Memory Write Cursor is not visible. 1 : Font write cursor/ Memory Write Cursor is visible.	0	RW
5	Font Write Cursor/ Memory Write Cursor Blink Enable 0 : Normal display. 1 : Blink display.	0	RW
4	NA	0	RO
3-2	Memory Write Direction (Only for Graphic Mode) 00b : Left → Right then Top → Down. 01b : Right → Left then Top → Down. 10b : Top → Down then Left → Right. 11b : Down → Top then Left → Right.	0	RW
1	Memory Write Cursor Auto-Increase Disable 0 : Cursor auto-increases when memory write. 1 : Cursor doesn't auto-increases when memory write.	0	RW
0	Memory Read Cursor Auto-Increase Disable 0 : Cursor auto-increases when memory read. 1 : Cursor doesn't auto-increases when memory read.	0	RW

REG[41h] Memory Write Control Register 1 (MWCR1)

Bit	Description	Default	Access
7	Graphic Cursor Enable 0 : Graphic Cursor disable. 1 : Graphic Cursor enable.	0	RW
6-4	Graphic Cursor Selection Bit Select one from eight graphic cursor types.(000b to 111b) 000b : Graphic Cursor Set 1. 001b : Graphic Cursor Set 2. 010b : Graphic Cursor Set 3. :: 111b : Graphic Cursor Set 8.	0	RW
3-2	Write Destination Selection 00b : Layer 1~2. 01b : CGRAM. 10b : Graphic Cursor. 11b : Pattern. Note : When CGRAM is selected (01b), REG[21h] bit 7 must be set as "0".	0	RW
1	NA	0	RO
0	Layer No. for Read/Write Selection When resolution =< 480x400 or color depth = 8bpp: 0 : Layer 1. 1 : Layer 2. When resolution > 480x400 and color depth > 8bpp: NA, always writing to Layer 1.	0	RW

REG[44h] Blink Time Control Register (BTCR)

Bit	Description	Default	Access
7-0	Text Blink Time Setting (Unit: Frame) 00h : 1 frame time. 01h : 2 frames time. 02h : 3 frames time. : : : : FFh : 256 frames time.	0	RW

REG[45h] Memory Read Cursor Direction (MRCD)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Memory Read Direction (Only for Graphic Mode) 00b : Left → Right then Top → Down. 01b : Right → Left then Top → Down. 10b : Top → Down then Left → Right. 11b : Down → Top then Left → Right.	0	RW

REG[46h] Memory Write Cursor Horizontal Position Register 0 (CURH0)

Bit	Description	Default	Access
7-0	Memory Write Cursor Horizontal Location[7:0]	0	RW

REG[47h] Memory Write Cursor Horizontal Position Register 1 (CURH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Memory Write Cursor Horizontal Location[9:8]	0	RW

REG[48h] Memory Write Cursor Vertical Position Register 0 (CURV0)

Bit	Description	Default	Access
7-0	Memory Write Cursor Vertical Location[7:0]	0	RW

REG[49h] Memory Write Cursor Vertical Position Register 1 (CURV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Memory Write Cursor Vertical Location[8]	0	RW

REG[4Ah] Memory Read Cursor Horizontal Position Register 0 (RCURH0)

Bit	Description	Default	Access
7-0	Memory Read Cursor Horizontal Location[7:0]	0	RW

REG[4Bh] Memory Read Cursor Horizontal Position Register 1 (RCURH01)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Memory Read Cursor Horizontal Location[9:8]	0	RW

REG[4Ch] Memory Read Cursor Vertical Position Register 0 (RCURV0)

Bit	Description	Default	Access
7-0	Memory Read Cursor Vertical Location[7:0]	0	RW

REG[4Dh] Memory Read Cursor Vertical Position Register 1 (RCURV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Memory Read Cursor Vertical Location[8]	0	RW

REG[4Eh] Font Write Cursor and Memory Write Cursor Horizontal Size Register (CURHS)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Font Write Cursor Horizontal Size Setting[4:0] Unit : Pixel Note : When font is enlarged, the cursor setting will multiply the same times as the font enlargement.	7h	RW

REG[4Fh] Font Write Cursor Vertical Size Register (CURVS)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Font Write Cursor Vertical Size Setting[4:0] Unit : Pixel Note : When font is enlarged, the cursor setting will multiply the same times as the font enlargement.	0	RW

REG[50h] BTE Function Control Register 0 (BECR0)

Bit	Description	Default	Access
7	BTE Function Enable / Status Write 0 : No action. 1 : BTE function enable. Read 0 : BTE function is idle. 1 : BTE function is busy.	0	RW
6	BTE Source Data Select 0 : Block mode, the Source BTE is stored as a rectangular region of memory. 1 : Linear mode, the Source BTE is stored as a continuous block of memory.	0	RW
5	BTE Destination Data Type Select 0 : Block mode, the Destination BTE is stored as a rectangular region of memory. 1 : Linear mode, the Destination BTE is stored as a continuous block of memory.	0	RW
4-0	NA	0	RO

REG[51h] BTE Function Control Register1 (BECR1)

Bit	Description	Default	Access
7-5	BTE ROP Code Bit[3:0] ROP is the acronym for Raster Operation. Some of BTE operation code has to collocate with ROP for the detailed function. (Please refer to the Section 7-6)	0	RW
4-0	BTE Operation Code Bit[3:0] RA8875 includes a 2D BTE Engine, it can execute 13 BTE functions, the operation code range is from 1100b to 0000b and 1111b to 1101b are not used. Some of BTE Operation Code has to collocate with the ROP code for the advance function. (Please refer to the Section 7-6)	0	RW

REG[68h] Background Color Register for Transparent 1 (BGTR1)

Bit	Description	Default	Access
7-6	NA	0	RO
5-0	Foreground Color Green[5:0] If REG[10h] Bit[3:2] is set to 256 colors, the register only uses Bit[2:0]. If REG[10h] Bit[3:2] is set to 65K colors, the register uses Bit[5:0].	0	RW

REG[69h] Background Color Register for Transparent 2 (BGTR2)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Foreground Color Blue[4:0] If REG[10h] Bit[3:2] is set to 256 colors, the register only uses Bit[1:0]. If REG[10h] Bit[3:2] is set to 65K colors, the register uses Bit[4:0].	0	RW

REG[70h] Touch Panel Control Register 0 (TPCR0)

Bit	Description	Default	Access
7	Touch Panel Enable Bit 0 : Disable 1 : Enable	0	RW
6-4	TP Sample Time Adjusting 000b : Wait 512 system clocks period for ADC data ready. 001b : Wait 1024 system clocks period for ADC data ready. 010b : Wait 2048 system clocks period for ADC data ready. 011b : Wait 4096 system clocks period for ADC data ready. 100b : Wait 8192 system clocks period for ADC data ready. 101b : Wait 16384 system clocks period for ADC data ready. 110b : Wait 32768 system clocks period for ADC data ready. 111b : Wait 65536 system clocks period for ADC data ready.	0	RW
3	Touch Panel Wakeup Enable 0 : Disable the Touch Panel wake-up function. 1 : Touch Panel can wake-up the sleep mode.	0	RW
2-0	ADC Clock Setting 000b : System CLK 001b : (System CLK) / 2. 010b : (System CLK) x 4. 011b : (System CLK) / 8. 100b : (System CLK) x 16. 101b : (System CLK) / 32. 110b : (System CLK) / x64. 111b : (System CLK) / 128.	0	RW

REG[71h] Touch Panel Control Register 1 (TPCR1)

Bit	Description	Default	Access
7	N/A	0	RO
6	TP Manual Mode Enable 0 : Auto mode. 1 : Using the manual mode.	0	RW
5	TP ADC Reference Voltage Source 0 : Vref generated from internal circuit. No external voltage is needed. 1 : Vref from external source, 1/2 VDD is needed for ADC.	0	RW
4-3	NA	0	RO
2	De-bounce Circuit Enable for Touch Panel Interrupt 0: De-bounce circuit disable. 1: De-bounce circuit enable.	0	RW
1-0	Mode Selection for TP Manual Mode 00b : IDLE mode: Touch Panel in idle mode. 01b : Wait for TP event, Touch Panel event could cause the interrupt or be read from REG[F1h] Bit2. 10b : Latch X data, in the phase, X Data can be latched in REG[72h] and REG[74h]. 11b : Latch Y data, in the phase, Y Data can be latched in REG[73h] and REG[74h].	0	RW

REG[72h] Touch Panel X High Byte Data Register (TPXH)

Bit	Description	Default	Access
7-0	Touch Panel X Data Bit[9:2]	0	RW

REG[73h] Touch Panel Y High Byte Data Register (TPYH)

Bit	Description	Default	Access
7-0	Touch Panel Y Data Bit[9:2]	0	RW

REG[74h] Touch Panel X/Y Low Byte Data Register (TPXYL)

Bit	Description	Default	Access
7	ADET Touch Event Detector 0 : Touch Panel is touched. 1 : Touch Panel is not touched.	1	RO
6-4	NA	0	RO
3-2	Touch Panel Y Data Bit[1:0]	0	RW
1-0	Touch Panel X Data Bit[1:0]	0	RW

REG[80h] Graphic Cursor Horizontal Position Register 0 (GCHP0)

Bit	Description	Default	Access
7-0	Graphic Cursor Horizontal Location[7:0]	0	RW

REG[81h] Graphic Cursor Horizontal Position Register 1 (GCHP1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Graphic Cursor Horizontal Location[9:8]	0	RW

REG[82h] Graphic Cursor Vertical Position Register 0 (GCVPO)

Bit	Description	Default	Access
7-0	Graphic Cursor Vertical Location[7:0]	0	RW

REG[83h] Graphic Cursor Vertical Position Register 1 (GCVP1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Graphic Cursor Vertical Location[8]	0	RW

REG[84h] Graphic Cursor Color 0 (GCC0)

Bit	Description	Default	Access
7-0	Graphic Cursor Color 0 with 256 colors RGB Format [7:0] = RRRGGGBB.	0	RW

REG[85h] Graphic Cursor Color 1 (GCC1)

Bit	Description	Default	Access
7-0	Graphic Cursor Color 1 with 256 Colors RGB Format [7:0] = RRRGGGBB.	0	RW

REG[88h] PLL Control Register 1 (PLL1)

Bit	Description	Default	Access
7	PLLDIVM PLL Pre-driver parameter. 0 : divided by 1. 1 : divided by 2.	0	RW
6-5	NA	0	RO
4-0	PLLDIVN[4:0] PLL input parameter, the value should be 1~31. (i.e. value 0 is forbidden).	0	RW

REG[89h] PLL Control Register 2 (PLL2)

Bit	Description	Default	Access
7-3	NA	0	RO
2-0	PLLDIVK[2:0] PLL Output divider 000b : divided by 1. 001b : divided by 2. 010b : divided by 4. 011b : divided by 8. 100b : divided by 16. 101b : divided by 32. 110b : divided by 64. 111b : divided by 128.	03h	RW

REG[8Ah] PWM1 Control Register (P1CR)

Bit	Description	Default	Access																
7	PWM1 Enable 0 : Disable, PWM1_OUT level depends on P1CR bit6. 1 : Enable.	0	RW																
6	PWM1 Disable Level 0 : PWM1_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM1_OUT is Normal H when PWM disable or Sleep mode. The bit is only usable when P1CR bit 4 is 0	0	RW																
5	Reserved	0	RO																
4	PWM1 Function Selection 0 : PWM1 function. 1 : PWM1 output a fixed frequency signal and it is equal to 1 /16 oscillator clock. PWM1 = Fosc / 16(Note)	0	RW																
3-0	PWM1 Clock Source Divide Ratio <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td>0000b : SYS_CLK / 1</td> <td>1000b : SYS_CLK / 256</td> </tr> <tr> <td>0001b : SYS_CLK / 2</td> <td>1001b : SYS_CLK / 512</td> </tr> <tr> <td>0010b : SYS_CLK / 4</td> <td>1010b : SYS_CLK / 1024</td> </tr> <tr> <td>0011b : SYS_CLK / 8</td> <td>1011b : SYS_CLK / 2048</td> </tr> <tr> <td>0100b : SYS_CLK / 16</td> <td>1100b : SYS_CLK / 4096</td> </tr> <tr> <td>0101b : SYS_CLK / 32</td> <td>1101b : SYS_CLK / 8192</td> </tr> <tr> <td>0110b : SYS_CLK / 64</td> <td>1110b : SYS_CLK / 16384</td> </tr> <tr> <td>0111b : SYS_CLK / 128</td> <td>1111b : SYS_CLK / 32768</td> </tr> </tbody> </table> For example, if the system clock is 20MHz and Bit[3:0] =0001b, when the clock source of PWM1 is 10MHz.	0000b : SYS_CLK / 1	1000b : SYS_CLK / 256	0001b : SYS_CLK / 2	1001b : SYS_CLK / 512	0010b : SYS_CLK / 4	1010b : SYS_CLK / 1024	0011b : SYS_CLK / 8	1011b : SYS_CLK / 2048	0100b : SYS_CLK / 16	1100b : SYS_CLK / 4096	0101b : SYS_CLK / 32	1101b : SYS_CLK / 8192	0110b : SYS_CLK / 64	1110b : SYS_CLK / 16384	0111b : SYS_CLK / 128	1111b : SYS_CLK / 32768	0	RW
0000b : SYS_CLK / 1	1000b : SYS_CLK / 256																		
0001b : SYS_CLK / 2	1001b : SYS_CLK / 512																		
0010b : SYS_CLK / 4	1010b : SYS_CLK / 1024																		
0011b : SYS_CLK / 8	1011b : SYS_CLK / 2048																		
0100b : SYS_CLK / 16	1100b : SYS_CLK / 4096																		
0101b : SYS_CLK / 32	1101b : SYS_CLK / 8192																		
0110b : SYS_CLK / 64	1110b : SYS_CLK / 16384																		
0111b : SYS_CLK / 128	1111b : SYS_CLK / 32768																		

Note : FOSC is the frequency of external oscillator.

REG[8Bh] PWM1 Duty cycle Register (P1DCR)

Bit	Description	Default	Access
7-0	PWM Cycle Duty Selection Bit 00h → 1 / 256 Duty with PWM1 clock source. 01h → 2 / 256 Duty with PWM1 clock source. 02h → 3 / 256 Duty with PWM1 clock source. : : FEh → 255 / 256 Duty with PWM1 clock source. FFh → 256 / 256 Duty with PWM1 clock source.	0	RW

REG[8Ch] PWM2 Control Register (P2CR)

Bit	Description	Default	Access																
7	PWM2 Enable 0 : Disable, PWM_OUT level depends on P2CR bit6. 1 : Enable.	0	RW																
6	PWM2 Disable Level 0 : PWM2_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM2_OUT is Normal H when PWM disable or Sleep mode. The bit is only usable when P2CR bit 4 is 0	0	RW																
5	Reserved	0	RO																
4	PWM2 Function Selection 0 : PWM2 function. 1 : PWM2 output a signal which is the same with system clock. PWM2 = SYS_CLK / 16 .	0	RW																
3-0	PWM2 Clock Source Divide Ratio <table border="1"> <tbody> <tr> <td>0000b : SYS_CLK / 1</td> <td>1000b : SYS_CLK / 256</td> </tr> <tr> <td>0001b : SYS_CLK / 2</td> <td>1001b : SYS_CLK / 512</td> </tr> <tr> <td>0010b : SYS_CLK / 4</td> <td>1010b : SYS_CLK / 1024</td> </tr> <tr> <td>0011b : SYS_CLK / 8</td> <td>1011b : SYS_CLK / 2048</td> </tr> <tr> <td>0100b : SYS_CLK / 16</td> <td>1100b : SYS_CLK / 4096</td> </tr> <tr> <td>0101b : SYS_CLK / 32</td> <td>1101b : SYS_CLK / 8192</td> </tr> <tr> <td>0110b : SYS_CLK / 64</td> <td>1110b : SYS_CLK / 16384</td> </tr> <tr> <td>0111b : SYS_CLK / 128</td> <td>1111b : SYS_CLK / 32768</td> </tr> </tbody> </table> For example, if the system clock is 20MHz and Bit[3:0] =0010b, then the clock source of PWM2 is 5MHz.	0000b : SYS_CLK / 1	1000b : SYS_CLK / 256	0001b : SYS_CLK / 2	1001b : SYS_CLK / 512	0010b : SYS_CLK / 4	1010b : SYS_CLK / 1024	0011b : SYS_CLK / 8	1011b : SYS_CLK / 2048	0100b : SYS_CLK / 16	1100b : SYS_CLK / 4096	0101b : SYS_CLK / 32	1101b : SYS_CLK / 8192	0110b : SYS_CLK / 64	1110b : SYS_CLK / 16384	0111b : SYS_CLK / 128	1111b : SYS_CLK / 32768	0	RW
0000b : SYS_CLK / 1	1000b : SYS_CLK / 256																		
0001b : SYS_CLK / 2	1001b : SYS_CLK / 512																		
0010b : SYS_CLK / 4	1010b : SYS_CLK / 1024																		
0011b : SYS_CLK / 8	1011b : SYS_CLK / 2048																		
0100b : SYS_CLK / 16	1100b : SYS_CLK / 4096																		
0101b : SYS_CLK / 32	1101b : SYS_CLK / 8192																		
0110b : SYS_CLK / 64	1110b : SYS_CLK / 16384																		
0111b : SYS_CLK / 128	1111b : SYS_CLK / 32768																		

REG[8Dh] PWM2 Control Register (P2DCR)

Bit	Description	Default	Access
7-0	PWM Cycle Duty Selection Bit 00h → 1 / 256 Duty with PWM2 clock source. 01h → 2 / 256 Duty with PWM2 clock source. 02h → 3 / 256 Duty with PWM2 clock source. : : FEh → 255 / 256 Duty with PWM2 clock source. FFh → 256 / 256 Duty with PWM2 clock source.	0	RW

REG[8Eh] Memory Clear Control Register (MCLR)

Bit	Description	Default	Access
7	Memory Clear Function 0 : End or Stop. When write 0 to this bit RA8875 will stop the Memory clear function. Or if read back this bit is 0, it indicates than Memory clear function is complete. 1 : Start the memory clear function.	0	RW
6	Memory Clear Area Setting 0 : Clear the full window. (Please refer to the setting of REG[14h], [19h], [1Ah]) 1 : Clear the active window(Please refer to the setting of REG[30h~37h]). The layer to be cleared is according to the setting REG[41h] Bit0.	0	RW
5-0	NA	0	RO

REG[90h] Draw Line/Circle/Square Control Register (DCR)

Bit	Description	Default	Access
7	Draw Line/Square/Triangle Start Signal Write Function 0 : Stop the drawing function. 1 : Start the drawing function. Read Function 0 : Drawing function complete. 1 : Drawing function is processing.	0	RW
6	Draw Circle Start Signal Write Function 0 : Stop the circle drawing function. 1 : Start the circle drawing function. Read Function 0 : Circle drawing function complete. 1 : Circle drawing function is processing.	0	RW
5	Fill the Circle/Square/Triangle Signal 0 : Non fill. 1 : Fill.	0	RW
4	Draw Line or Square Select Signal 0 : Draw line. 1 : Draw square.	0	RW
3-1	NA	0	RO
0	Draw Triangle or Line/Square Select Signal 0 : Draw Line or square 1 : Draw Triangle	0	RW

REG[91h] Draw Line/square Horizontal Start Address Register0 (DLHSR0)

Bit	Description	Default	Access
7-0	Draw Line/Square Horizontal Start Address[7:0]	0	RW

REG[92h] Draw Line/Square Horizontal Start Address Register1 (DLHSR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Line/Square Horizontal Start Address[9:8]	0	RW

REG[93h] Draw Line/Square Vertical Start Address Register0 (DLVSR0)

Bit	Description	Default	Access
7-0	Draw Line/Square Vertical Start Address[7:0]	0	RW

REG[94h] Draw Line/Square Vertical Start Address Register1 (DLVSR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Line/square Vertical Start Address[8]	0	RW

Note: start point and end point cannot equal.

REG[95h] Draw Line/Square Horizontal End Address Register0 (DLHER0)

Bit	Description	Default	Access
7-0	Draw Line/Square Horizontal End Address[7:0]	0	RW

REG[96h] Draw Line/Square Horizontal End Address Register1 (DLHER1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Line/Square Horizontal End Address[9:8]	0	RW

REG[97h] Draw Line/Square Vertical End Address Register0 (DLVER0)

Bit	Description	Default	Access
7-0	Draw Line/Square Vertical End Address[7:0]	0	RW

REG[98h] Draw Line/Square Vertical End Address Register1 (DLVER1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Line/Square Vertical End Address[8]	0	RW

Note: start point and end point cannot equal.

REG[99h] Draw Circle Center Horizontal Address Register0 (DCHR0)

Bit	Description	Default	Access
7-0	Draw Circle Center Horizontal Address[7:0]	0	RW

REG[9Ah] Draw Circle Center Horizontal Address Register1 (DCHR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Circle Center Horizontal Address[9:8]	0	RW

REG[9Bh] Draw Circle Center Vertical Address Register0 (DCVR0)

Bit	Description	Default	Access
7-0	Draw Circle Center Vertical Address[7:0]	0	RW

REG[9Ch] Draw Circle Center Vertical Address Register1 (DCVR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Circle Center Vertical Address[8]	0	RW

REG[9Dh] Draw Circle Radius Register (DCRR)

Bit	Description	Default	Access
7-0	Draw Circle Radius[7:0]	0	RW

REG[A0h] Draw Ellipse/Ellipse Curve/Circle Square Control Register

Bit	Description	Default	Access
7	Draw Ellipse/Circle Square start Signal Write Function 0 : Stop the drawing function. 1 : Start the drawing function. Read Function 0 : Drawing function complete. 1 : Drawing function is processing.	0	RW
6	Fill the Ellipse/Circle Square Signal 0 : Non fill. 1 : fill.	0	RW
5	Draw Ellipse/ Ellipse Curve or Circle Square Select Signal 0 : Draw Ellipse/ Ellipse curve.(Depend on bit4) 1 : Draw Circle Square.	0	RW
4	Draw Ellipse or Ellipse Curve Select Signal 0 : Draw Ellipse 1 : Draw Ellipse Curve	0	RW
3-2	NA	0	RO
1-0	Draw Ellipse Curve Part Select(DECP)	0	RW

REG[A1h] Draw Ellipse/Circle Square Long axis Setting Register (ELL_A0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Long axis[7:0]	0	RW

REG[A2h] Draw Ellipse/Circle Square Long axis Setting Register (ELL_A1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Ellipse/Circle Square Long axis[9:8]	0	RW

REG[A3h] Draw Ellipse/Circle Square Short axis Setting Register (ELL_B0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Short axis[7:0]	0	RW

REG[A4h] Draw Ellipse/Circle Square Short axis Setting Register (ELL_B1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Ellipse/Circle Square Short axis[8]	0	RW

REG[A5h] Draw Ellipse/Circle Square Center Horizontal Address Register0 (DEHR0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Center Horizontal Address[7:0]	0	RW

REG[A6h] Draw Ellipse/Circle Square Center Horizontal Address Register1 (DEHR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Ellipse/Circle Square Center Horizontal Address[9:8]	0	RW

REG[A7h] Draw Ellipse/Circle Square Center Vertical Address Register0 (DEVRO)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Center Vertical Address[7:0]	0	RW

REG[A8h] Draw Ellipse/Circle Square Center Vertical Address Register1 (DEV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Ellipse/Circle Square Center Vertical Address[8]	0	RW

REG[A9h] Draw Triangle Point 2 Horizontal Address Register0 (DTPH0)

Bit	Description	Default	Access
7-0	Draw Triangle Point 2 Horizontal Address[7:0]	0	RW

REG[AAh] Draw Triangle Point 2 Horizontal Address Register1 (DTPH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Triangle Point 2 Horizontal Address[9:8]	0	RW

REG[ABh] Draw Triangle Point 2 Vertical Address Register0 (DTPV0)

Bit	Description	Default	Access
7-0	Draw Triangle Point 2 Vertical Address [7:0]	0	RW

REG[ACh] Draw Triangle Point 2 Vertical Address Register1 (DTPV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Triangle Point 2 Vertical Address [8]	0	RW

REG[B0h] Source Starting Address REG0 (SSAR0)

Bit	Description	Default	Access
7-0	DMA Source START ADDRESS [7:0]	0	RW

REG[B1h] Source Starting Address REG 1 (SSAR1)

Bit	Description	Default	Access
7-0	DMA Source START ADDRESS [15:8]	0	RW

REG[B2h] Source Starting Address REG 2 (SSAR2)

Bit	Description	Default	Access
7-0	DMA Source START ADDRESS [23:16]	0	RW

REG[B4h] Block Width REG 0(BWR0) / DMA Transfer Number REG 0 (DTNR0)

Bit	Description	Default	Access
7-0	When REG[BFh] bit 1 = 0 (Continuous Mode) DMA Transfer Number [7:0] When REG[BFh] bit 1 = 1 (Block Mode) DMA Block Width [7:0]	0	RW

REG[B5h] Block Width REG 1 (BWR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	DMA Block Width [9:8]	0	RW

REG[B6h] Block Height REG 0(BHR0) /DMA Transfer Number REG 1 (DTNR1)

Bit	Description	Default	Access
7-0	When REG[BFh] bit 1 = 0 (Continuous Mode) DMA Transfer Number [15:8] When REG[BFh] bit 1 = 1 (Block Mode) DMA Block Height [7:0]	0	RW

REG[B7h] Block Height REG 1 (BHR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	DMA Block Height [9:8]	0	RW

REG[B8h] Source Picture Width REG 0(SPWR0) / DMA Transfer Number REG 2(DTNR2)

Bit	Description	Default	Access
7-3	DMA Source Picture Width [7:3]	0	RW
2-0	When REG[BFh] bit 1 = 0 (Continuous Mode) DMA Transfer Number [18:16] When REG[BFh] bit 1 = 1 (Block Mode) DMA Source Picture Width [2:0]	0	RW

REG[B9h] Source Picture Width REG 1 (SPWR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	DMA Source Picture Width [9:8]	0	RW

REG[BFh] DMA Configuration REG (DMACR)

Bit	Description	Default	Access
7-2	NA	0	RO
1	DMA Continuous or Block Read/Write Select Bit 0: Continuous / 1: Block	0	RW
0	Write Function→ DMA Start Bit Set to 1 by MCU and reset to 0 automatically Read Function→ DMA Busy Check Bit 0:Idle / 1:Busy	0	RW

REG [C0h] Key-Scan Control Register 1 (KSCR1)

Bit	Description	Default	Access																																																												
7	Key-Scan Enable Bit(KEY_EN) 1 : Enable. 0 : Disable.	0	RW																																																												
6	LongKey Enable Bit 1 : Enable. Long key period is set by KSCR2 bit4-2. 0 : Disable.	0	RW																																																												
5-4	Key-Scan Data Sampling Times De-bounce times of scan frequency. 00b : 4 01b : 8 10b : 16 11b : 32	0	RW																																																												
3	NA		RO																																																												
2-0	KF2-0: Key-Scan Frequency	0	RW																																																												
	<table border="1"> <thead> <tr> <th>KF2</th> <th>KF1</th> <th>KF0</th> <th colspan="3">KF0 Key-Scan Cycle (4x5)</th> </tr> <tr> <th colspan="3">System Clock</th> <th>20MHz</th> <th>40MHz</th> <th>60MHz</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>128μs</td> <td>64μs</td> <td>42.67us</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>256μs</td> <td>128μs</td> <td>85.33μs</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>512μs</td> <td>256μs</td> <td>170.67μs</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1.024ms</td> <td>512μs</td> <td>341.33μs</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>2.048ms</td> <td>1.024ms</td> <td>682.67us</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>4.096ms</td> <td>2.048ms</td> <td>1.365ms</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>8.192ms</td> <td>4.096ms</td> <td>2.731ms</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>16.384ms</td> <td>8.192ms</td> <td>5.461ms</td> </tr> </tbody> </table>			KF2	KF1	KF0	KF0 Key-Scan Cycle (4x5)			System Clock			20MHz	40MHz	60MHz	0	0	0	128μs	64μs	42.67us	0	0	1	256μs	128μs	85.33μs	0	1	0	512μs	256μs	170.67μs	0	1	1	1.024ms	512μs	341.33μs	1	0	0	2.048ms	1.024ms	682.67us	1	0	1	4.096ms	2.048ms	1.365ms	1	1	0	8.192ms	4.096ms	2.731ms	1	1	1	16.384ms	8.192ms	5.461ms
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REG [C1h] Key-Scan Controller Register 2 (KSCR2)

Bit	Description	Default	Access																				
7	Key-Scan Wakeup Function Enable Bit 0: Key-Scan Wakeup function is disable. 1: Key-Scan Wakeup function is enable.	0	RW																				
6-4	NA	0	RO																				
3-2	Long Key Timing Adjustment	0	RW																				
	<table border="1"> <thead> <tr> <th>System Clock</th> <th>20MH</th> <th>40MHz</th> <th>60MHz</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1.25 sec</td> <td>0.625 sec</td> <td>0.3125 sec</td> </tr> <tr> <td>01b</td> <td>2.5 sec</td> <td>1.25 sec</td> <td>0.625 sec</td> </tr> <tr> <td>10b</td> <td>3.75 sec</td> <td>1.875 sec</td> <td>0.9375 sec</td> </tr> <tr> <td>11b</td> <td>5 sec</td> <td>2.5 sec</td> <td>1.25 sec</td> </tr> </tbody> </table>			System Clock	20MH	40MHz	60MHz	00b	1.25 sec	0.625 sec	0.3125 sec	01b	2.5 sec	1.25 sec	0.625 sec	10b	3.75 sec	1.875 sec	0.9375 sec	11b	5 sec	2.5 sec	1.25 sec
	System Clock			20MH	40MHz	60MHz																	
	00b			1.25 sec	0.625 sec	0.3125 sec																	
	01b			2.5 sec	1.25 sec	0.625 sec																	
10b	3.75 sec	1.875 sec	0.9375 sec																				
11b	5 sec	2.5 sec	1.25 sec																				
1-0	Numbers of Key Hit. 00b : No key is pressed 01b : One key is pressed, read REG[C2h] for the key code. 10b : Two keys are pressed, read REG[C2h ~ C3h] for the key codes. 11b : Three keys are pressed, read REG[C2h ~ C4h] for the key codes.	0	RO																				

REG [C2h] Key-Scan Data Register (KSDR0)

Bit	Description	Default	Access
7-0	Key Strobe Data0 The corresponding key code 0 that is pressed. Please refer to section 7-9 for detail description.	NA	RO

REG [C3h] Key-Scan Data Register (KSDR1)

Bit	Description	Default	Access
7-0	Key Strobe Data1 The corresponding key code 1 that is pressed. Please refer to section 7-9 for detail description.	NA	RO

REG [C4h] Key-Scan Data Register (KSDR2)

Bit	Description	Default	Access
7-0	Key Strobe Data2 The corresponding key code 2 that is pressed. Please refer to section 7-9 for detail description.	NA	RO

REG[C7h] Extra General Purpose IO Register (GPIOX)

Bit	Description	Default	Access
7-1	NA	0	RO
0	The GPIX/GPOX Data Bit Read: Input data from GPIX pin. Write: Output data to GPOX pin.	NA	RW

Registers REG [D0h] Floating Windows Start Address XA 0 (FWSAXA0)

Bit	Description	Default	Access
7-0	Floating Windows Start Address XA [7:0]	0	RW

REG [D1h] Floating Windows Start Address XA 1 (FWSAXA1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Floating Windows Start Address XA [9:8]	0	RW

REG [D2h] Floating Windows Start Address YA 0 (FWSAYA0)

Bit	Description	Default	Access
7-0	Floating Windows Start Address YA [7:0]	0	RW

REG [D3h] Floating Windows Start Address YA 1 (FWSAYA1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Floating Windows Start Address YA [8]	0	RW

REG [D4h] Floating Windows Width 0 (FWW0)

Bit	Description	Default	Access
7-0	Floating Windows Width Setting [7:0]	0	RW

REG [D5h] Floating Windows Width 1 (FWW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Floating Windows Width Setting [9:8]	0	RW

REG [D6h] Floating Windows Height 0 (FWH0)

Bit	Description	Default	Access
7-0	Floating Windows Height Setting[7:0]	0	RW

REG [D7h] Floating Windows Height 1 (FWH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Floating Windows Height Setting [9:8]	0	RW

REG [D8h] Floating Windows Display X Address 0 (FWDXA0)

Bit	Description	Default	Access
7-0	Floating Windows Display X Address [7:0]	0	RW

REG [D9h] Floating Windows Display X Address 1 (FWDXA1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Floating Windows Display X Address [9:8]	0	RW

REG [DAh] Floating Windows Display Y Address 0 (FWDYA0)

Bit	Description	Default	Access
7-0	Floating Windows Display X Address [7:0]	0	RW

REG [DBh] Floating Windows Display Y Address 1 (FWDYA1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Floating Windows Display Y Address [8]	0	RW

SACS_MODE REG [E0h] Serial Flash/ROM Direct Access Mode

Bit	Description	Default	Access
7-1	NA	0	RO
0	0: direct access mode disable, then user can use for FONT/DMA mode. 1: direct access mode enable, then FONT/DMA mode disable	0	RW

SACS_ADDR REG [E1h] Serial Flash/ROM Direct Access Mode Address

Bit	Description	Default	Access
7-0	Direct access mode Address Serial Flash/ROM have 24 bit address data, user must be write 3 times E1 for address setting.	0	WO

SACS_DATA [E2h] Serial Flash/ROM Direct Access Data Read

Bit	Description	Default	Access
7-0	Direct access mode Read Data buffer	0	RO

REG[F0h] Interrupt Control Register1 (INTC1)

Bit	Description	Default	Access
7-5	NA	0	RO
4	KEYSCAN Interrupt Enable Bit 0 : Disable KEYSKAN interrupt. 1 : Enable KEYSKAN interrupt.	0	RW
3	DMA Interrupt Enable Bit 0 : Disable DMA interrupt. 1 : Enable DMA interrupt.	0	RW
2	Touch Panel Interrupt Enable Bit 0 : Disable Touch interrupt. 1 : Enable Touch interrupt.	0	RW
1	BTE Process complete Interrupt Enable Bit 0 : Disable BTE process complete interrupt. 1 : Enable BTE process complete interrupt.	0	RW
0	When MCU-relative BTE operation is selected(*1) and BTE Function is Enabled(REG[50h] Bit7 = 1), this bit is used to Enable the BTE Interrupt for MCU R/W: 0 : Disable BTE interrupt for MCU R/W. 1 : Enable BTE interrupt for MCU R/W. When the BTE Function is disabled, this bit is used to Enable the Interrupt of Font Write Function: 0 : Disable font write interrupt. 1 : Enable font write interrupt.	0	RW

Note : 1. MCU-relative BTE operations include "Write BTE with ROP", "Read BTE", "Transparent Write BTE", "Color Expand", "Color Expand with Transparency".

2. Font Write Interrupt indicates the completion of the font character writing to the DDRAM.

REG[F1h] Interrupt Control Register2 (INTC2)

Bit	Description	Default	Access
7-5	NA	0	RO
4	<p>Write Function → KEYSKAN Interrupt Clear Bit 0 : No operation. 1 : Clear the keyscan interrupt.</p> <p>Read Function → KEYSKAN Interrupt Status 0 : No keyscan interrupt happens. 1 : Keyscan interrupt happens.</p>	0	RW
3	<p>Write Function → DMA Interrupt Clear Bit 0 : No operation. 1 : Clear the DMA interrupt.</p> <p>Read Function → DMA Interrupt Status 0 : No DMA interrupt happens. 1 : DMA interrupt happens.</p>	0	RW
2	<p>Write Function → Touch Panel Interrupt Clear Bit 0 : No operation. 1 : Clear the touch interrupt.</p> <p>Read Function → Touch Panel Interrupt Status 0 : No Touch Panel interrupt happens. 1 : Touch Panel interrupt happens.</p>	0	RW
1	<p>Write Function → BTE Process Complete Interrupt Clear Bit 0 : No operation. 1 : Clear BTE process complete interrupt.</p> <p>Read Function → BTE Interrupt Status 0 : No BTE process complete interrupt happens. 1 : BTE process complete interrupt happens.</p>	0	RW
0	<p>When MCU-relative BTE operation is selected (*1) and BTE Function is Enabled (REG[50h] Bit7 = 1) Write Function → BTE Interrupt for MCU R/W Enable Bit 0 : No operation. 1 : Clear BTE MCU R/W interrupt.</p> <p>Read Function → BTE R/W Interrupt Status 0 : No BTE interrupt for MCU R/W happens. 1 : BTE interrupt for MCU R/W happens.</p> <p>When BTE is not Enable and Text Mode is Enable Write Function → Font Write Interrupt (*2) Enable Bit 0 : No operation. 1 : Clear font write interrupt.</p> <p>Read Function → Font Write Interrupt Status 0 : No font write interrupt happens. 1 : Font write interrupt happens.</p>	0	RW

Note:

Please refer to RA8875 data sheet for details

8. Optical Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle	θ_T	(CR \geq 10)	40	50	-	degree	Note 2
	θ_B		60	70	-		
	θ_L		60	70	-		
	θ_R		60	70	-		
Contrast ratio	CR	$\theta=0^\circ$	500	600	-	-	Note 1,3
Response Time	T _{on}	25°C	-	20	30	msec	Note 1,4
	T _{off}		-	-	-	msec	
Chromaticity	White	Backlight is on	X	0.260	0.310	0.360	Note 1,5
			Y	0.280	0.330	0.380	
	Red		X	0.540	0.590	0.640	
			Y	0.300	0.350	0.400	
	Green		X	0.298	0.348	0.398	
			Y	0.520	0.570	0.620	
	Blue		X	0.095	0.145	0.195	
			Y	0.060	0.110	0.160	
Luminance	L		-	200	-	cd/m ²	Note 1,6
NTSC			-	50	-	%	Note 5
Luminance uniformity	U		75	80	-	%	Note 1,7

Test Conditions:

1. IF= 40 mA, VF=23.1V, and the ambient temperature is 25. °C
2. The test systems refer to Note 1 and Note 2.

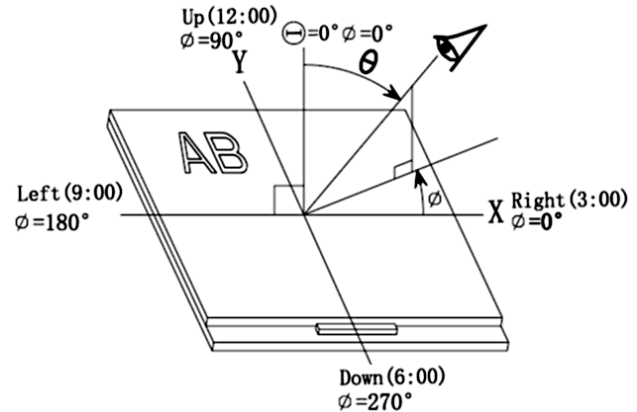
Note 1:

The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment SR-3A (1°) Measuring condition:

- Measuring surroundings: Dark room
- Measuring temperature: Ta=25°C.
- Adjust operating voltage to get optimum contrast at the center of the display.

Note 2:

The definition of viewing angle: Refer to the graph below marked by θ and ϕ



Note 3:

The definition of contrast ratio (Test LCM using SR-3A (1°)):

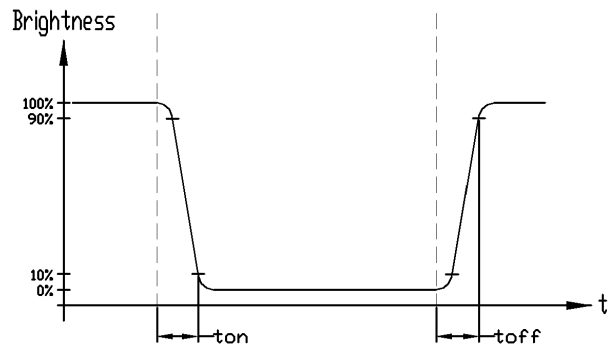
$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

Note 4:

Definition of Response time. (Test LCD using BM-7A(2°)):

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

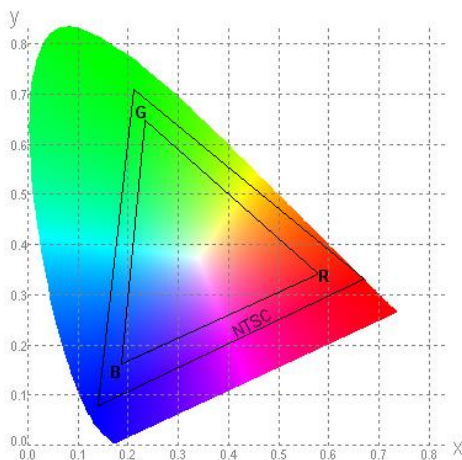


Note 5:

Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



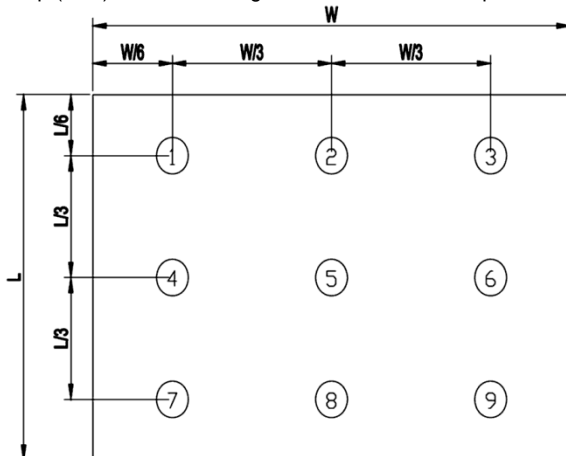
Note 6:

The luminance uniformity is calculated by using following formula.

$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.



Note 7:

Measured the luminance of white state at center point

9. LCD Module Design and Handling Precautions

- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.
- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may come out under abnormal contrast ratio.
- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply.
- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.
- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).
- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0 C~40 C <80%RH.
- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.
- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module. (eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.
- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.
- Never add force to components of LCD module. It may cause invisible damage or degrade the module's reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.
- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.

9. 液晶显示模块设计和使用须知

- 请注意 V0, VCOM 的设定, 以确保液晶显示模块在不同的使用温度下以及在不同的视角和位置观察模块显示, 均能达到最佳对比度, 请务必将应用电路上设置为对比度可调。
- 请注意液晶显示模块的显示品质判定是指在正常对比度下以及视窗 (V. A) 范围内进行的, 非正常对比度下液晶可能会出现非预期的显示不良, 应注意区分。
- 请勿在最大额定值以外使用液晶显示模块。
- 请勿在没有接通电源的条件下, 给液晶显示模块输送信号。
- 请尽可能缩短信号线的连接, 以避免对液晶显示模块的信号干扰。
- 集成电路因 IC 芯片 (如 TAB 或 COG) 对紫外线极为敏感, 强光环境下可能会引起液晶显示模块功能失效, 故应采用不透光的外壳。
- 请在液晶显示模块与外壳之间保留足够的空间 (可使用衬垫), 以缓冲外力对液晶显示模块的损坏或因受力不均而产生的显示不匀等异常现象。
- 避免液晶显示屏在某一画面下长时间点亮, 否则有出现残影的风险; 请通过软件每隔一段时间改变一次画面。
- 液晶显示模块的可靠性可能因温度冲击而降低。
- 请勿在阳光直射、高湿、高温或低温下储存和使用液晶显示模块, 这将造成液晶显示模块的损坏或失效。
- 请勿在极限环境 (最大/最小存储/工作温度) 下使用或放置液晶显示模块超过 48 小时以上。
- 液晶显示模块建议存储条件为: 0 C~40 C <80%RH。
- 请勿让液晶显示模块存储于带有酸性、碱性、有害气体环境之中。
- 在运输过程中, 请勿让液晶显示模块跌落与猛烈震动, 同时避免异常挤压, 高湿度, 与阳光照射。
- 液晶显示模块极易受静电损坏, 请务必保证液晶显示模块在防静电的工作环境中使用或保存。(如: 烙铁正确接地, 等)
- 拿取液晶显示模块时需注意操作人员的接地情况。
- 请手持液晶显示模块的边沿取放模块, 防止热压纸或 TAB 部位受力。
- 焊接液晶模块时, 请注意控制烙铁的温度、焊接时间, 以免烫坏导光板或偏光片, 导致显示不匀等不良现象发生。
- 请勿使用洗板水等腐蚀性液体接触液晶模块, 以免腐蚀导光板或模块电路。
- 仅可使用柔软的干布, 异丙醇或乙醇清洁液晶屏表面, 其他任何溶剂 (如: 水) 都有可能损坏液晶模块。
- 请勿挤压液晶显示模块上的元器件, 以避免产生潜在的损坏或失效而影响产品可靠性。
- 装配液晶显示模块时, 请务必注意避免液晶显示模块的扭曲或变形。
- 请勿挤压液晶显示屏表面, 这将导致显示颜色的异常。
- 液晶屏由玻璃制作而成, 任何机械碰撞 (如从高处跌

- LCD panel is made with glass. Any mechanical shock (e.g. dropping from high place) will damage the LCD module.
- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.
- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.
- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.
- LCD panel has sharp edges, please handle with care.
- Never attempt to disassemble or rework LCD module.
- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.

落)均有可能损坏液晶显示模块。

- 液晶屏表面带有保护膜，揭除保护膜时需要注意可能产生的静电。
- 因液晶显示屏表面的偏光片极易划伤，安装完成之前请尽量不要揭下保护膜。
- 请缓慢揭除保护膜，在此过程中液晶显示屏上可能会产生静电，此为正常情况，可在短时间内消失。
- 请注意避免被液晶显示屏的边缘割伤。
- 请不要试图拆卸或改造液晶显示模块。
- 当液晶显示屏出现破裂，内部液晶液体可能流出；相关液体不可吞吃，绝对不可接触嘴巴，如接触到皮肤或衣服，请使用肥皂与清水彻底清洗。

10. CTP Mounting Instructions

10. 电容触摸屏安装指导

10.1 Bezel Mounting (Figure 1)

10.1 面框安装 (附图 1)

- The bezel window should be bigger than the CTP active area. It should be $\geq 0.5\text{mm}$ each side.
- Gasket should be installed between the bezel and the CTP surface. The final gap should be about 0.5~1.0mm.
- It is recommended to provide an additional support bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

- 客户面框窗口应大于 CTP 动作区域，各边离动作区应 $\geq 0.5\text{mm}$ 。
- 面框与 CTP 面板间应垫有胶垫，其最终间隙约为 0.5~1.0mm。
- 建议必要时在背面提供附加支架 (例如无安装结构的薄型 TFT 模块)，应仅利用适当支撑以保持模块位置。
- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上。

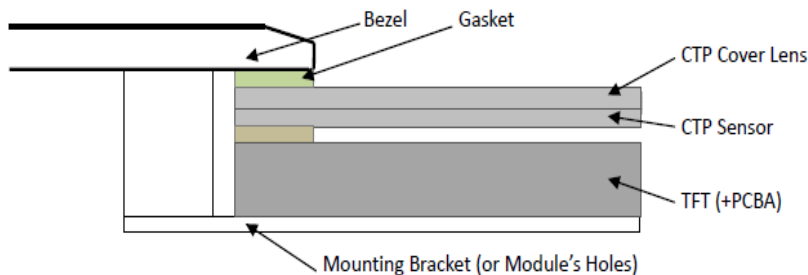


Figure 1

10.2 Surface Mounting (Figure 2)

10.2 嵌入安装 (附图 2)

- As the CTP assembling on the countersink area with double side adhesive. The countersink area should be flat and clean to ensure the double side adhesive installation result.
- The Bezel is recommend to keep a gap ($\geq 0.3\text{mm}$ each side) around the cover lens for tolerance.
- It is recommended to provide an additional support bracket with gasket for backside support when necessary (e.g. TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module

- 客户面框应具有使用双面胶粘贴 CTP 的结构沉台面，其粘贴面要求平整且洁净无污以保证粘贴牢靠。
- 考虑到制作误差，建议面框与 CTP 盖板之间四周留有 $\geq 0.3\text{mm}$ 间隙。
- 建议必要时在背面提供垫有胶垫附加支架 (例如无安装结构的 TFT 模块)，应仅利用适当支撑以保持模块位置。
- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上。

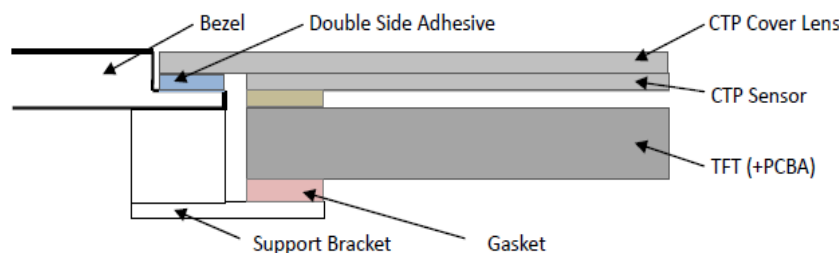


Figure 2

10.3 Additional Cover Lens Mounting (Figure 3)

- For the case of additional cover Lens mounting, it is necessary to recheck with the CTP specification about the material and thickness to ensure the functionality.
- It should keep a 0.2~0.3mm gap between the cover lens and the CTP surface..
- The cover lens window should be bigger than the active area of the CTP.It should be $\geq 0.5\text{mm}$ each side.
- It is recommended to provide an additional support bracket for backside support when necessary (e.g. slim type TFT module without mounding structure). They should only provide appropriate support and keep the module in place.
- The mounting structure should be strong enough to prevent external uneven force or twist act onto the module.

10.3 覆加盖板（附图3）

- 需要覆加玻璃盖板的安装，为确保其功能，有必要查看产品规格书中有关盖板材料和厚度的说明。
- 玻璃盖板与CTP表面之间应留有0.2~0.3mm间隙。
- 玻璃盖板视窗应大于CTP动作区域，各边离动作区应 $\geq 0.5\text{mm}$ 。
- 建议必要时在背面提供附加支架(例如无安装结构的薄型TFT模块)，应仅利用适当支撑以保持模块位置。
- 安装结构应具有足够的强度，以防止外部不均匀力或扭曲力作用到模块上。

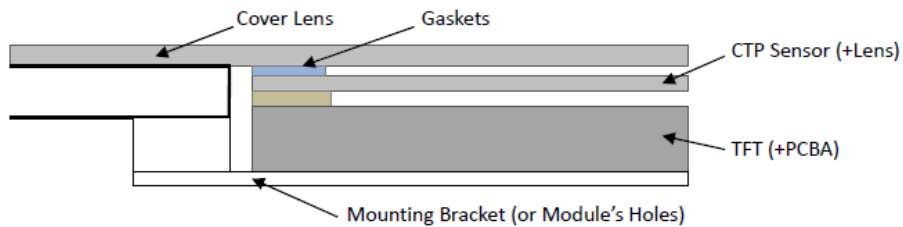


Figure 3

11. RTP Mounting Instructions

- It should bezel touching the RTP Active Area (A.A.) to prevent abnormal touch.It should left gab $D=0.2\sim 0.3\text{mm}$ in between. (Figure 4)
- Outer bezel design should take care about the area outside the A.A. Those areas contain circuit wires which is having different thickness. Touching those areas could de-form the ITO film. As a result bezel the ITO film be damaged and shorten its lifetime. It is suggested to protect those areas with gasket (between the bezel and RTP).The suggested figures are $B\geq 0.50\text{mm}$; $C\geq 0.50\text{mm}$. (Figure 4)
- The bezel side wall should keep space $E= 0.2 \sim 0.3\text{mm}$ from the RTP. (Figure 4)

11. 电阻触摸屏安装指导

- 为避免面框直接压在动作区(A.A.)上造成误动作，面框与电阻触摸屏(RTP)之间应留有一定的空隙 $D=0.2\sim 0.3\text{mm}$ 之间。(附图4)
- 设计面框时，要注意用面框保护触摸屏四周的非保证操作区域，因为布线区域在此处形成一台阶，在此区域附近操作时ITO Film变形较大，容易导致ITO损坏而降低寿命。为保护RTP和避免误操作，在RTP与面框之间垫缓冲物(Gasket)，我们建议设计面框应覆盖动作区的边缘，面框边缘到V.A.区的距离 $B\geq 0.50\text{mm}$ ；垫圈内边缘到V.A.区的距离 $C\geq 0.50\text{mm}$ 。(附图4)
- 在设计面框与RTP组装时，应考虑到面框内侧与RTP外侧的间距 $E\geq 0.2\text{mm}$ 。(附图4)

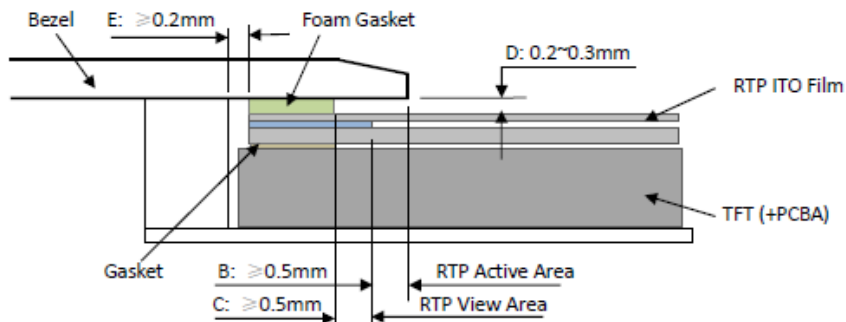


Figure 4

- In general design, RTP V.A. should be bigger than the TFT V.A. and RTP A.A. should be bigger than the TFT A.A. (Figure 5)

- 通常设计时：RTP的可视区V.A.应不小于TFT的可视区V.A.及RTP的动作区A.A.应不小于TFT的动作区A.A. (附图5)

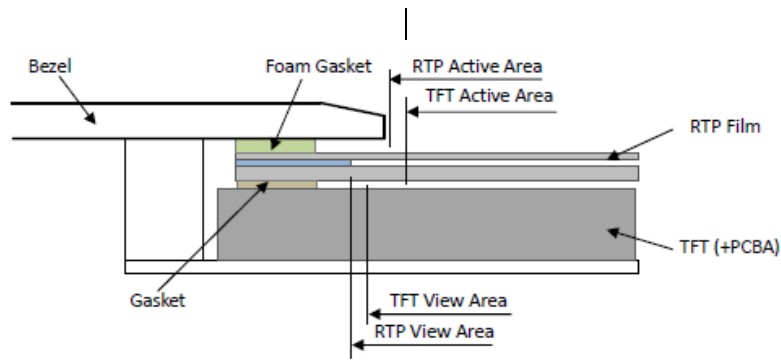
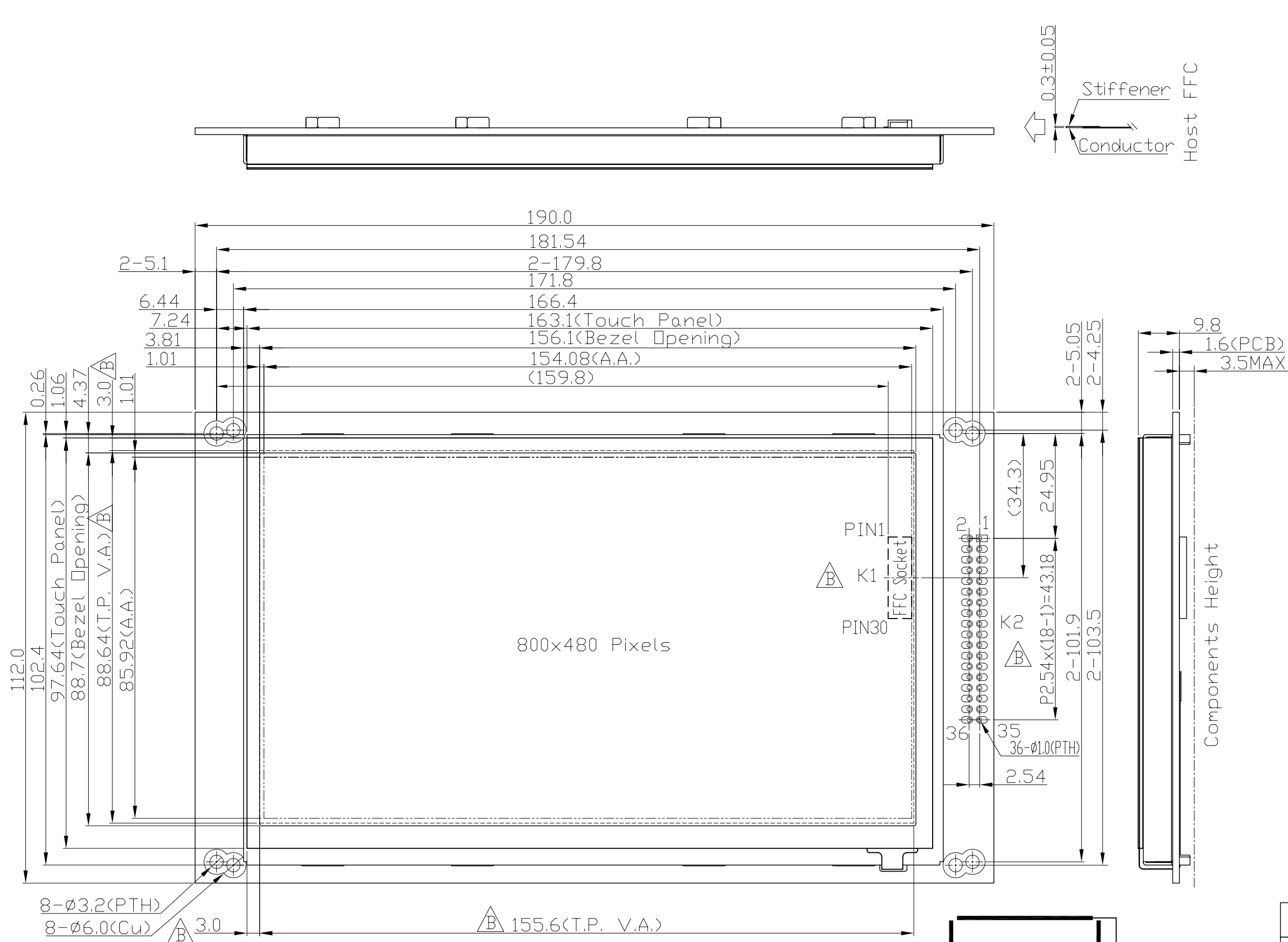


Figure 5

Warranty

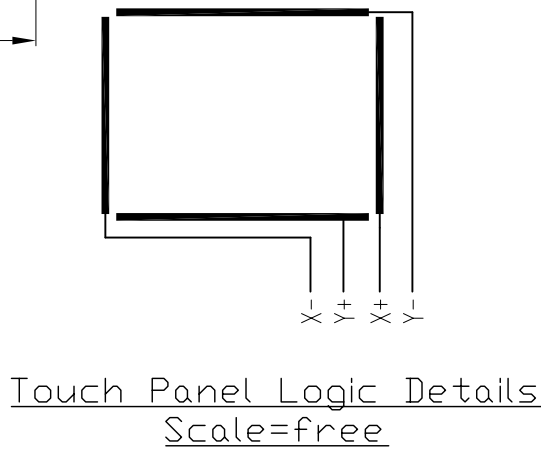
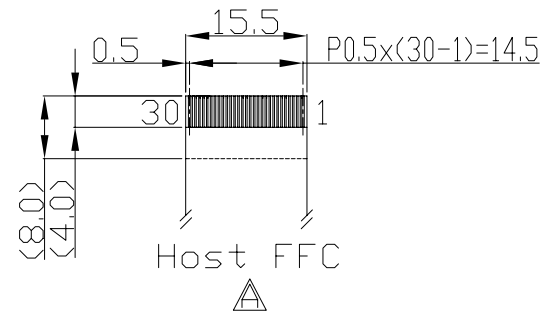
This product has been manufactured to our company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed our company's acceptance inspection procedures.
- When the product is in CCFL models, CCFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- We cannot accept responsibility for intellectual property of a third part, which may arise through the application of our product to our assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.



Terminal(K2)		Terminal(K1)	
No	Name	No	Name
1	VDD(5V)	1	VSS(0V)
2	VDD(5V)	2	VDD(5V)
3	VDD(5V)	3	VDD(5V)
4	VDD(5V)	4	RS
5	VSS(0V)	5	/WR
6	VSS(0V)	6	/RD
7	/WR	7	/CS
8	/RD	8	VSS(0V)
9	/CS	9	/WAIT
10	RS	10	/INT
11	DB15	11	/RST
12	DB14	12	DB0
13	DB13	13	DB1
14	DB12	14	DB2
15	DB11	15	DB3
16	DB10	16	DB4
17	DB9	17	DB5
18	DB8	18	DB6
19	DB7	19	DB7
20	DB6	20	VSS(0V)
21	DB5	21	VDD(5V)
22	DB4	22	VSS(0V)
23	DB3	23	DB8
24	DB2	24	DB9
25	DB1	25	DB10
26	DB0	26	DB11
27	VSS(0V)	27	DB12
28	VSS(0V)	28	DB13
29	/INT	29	DB14
30	/WAIT	30	DB15
31	NC		
32	/RST		
33	NC		
34	NC		
35	VSS(0V)		
36	VSS(0V)		

- Note:
- *1. LCD Display Type: TFT.Transmissive
 - *2. Pixel Arrangement: RGB-STRIPE
 - *3. Color Depth: 65k colors
 - *4. Operating Voltage: 5.0V \triangle
 - *5. Backlight: LEDs
 - *6. Touch Panel Type : Resistive Touch Panel
 - *7. Operating Temperature: -20°C~70°C
 - *8. Storage Temperature: -30°C~80°C
 - *9. Foam Gasket must be assemble outside TP VA by 0.5mm \triangle



B	-Revise Outline	Chen Ji
		2016-03-18
A	-Typing Correction	Zou Guo Rui
	-Refine Outline	2015-07-15
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Scale 1/1	Tol. ±0.5	Unit mm Paper Size A3
Approved	Checked	Drawn Zou Guo Rui

TOPWAY